AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended): A method of forming a photo sensor in a photo diode formed on a semiconductor wafer, a surface of the semiconductor comprising a substrate with first-type dopants, and an insulating layer positioned on ~~a surface~~ the surface of the substrate and surrounding the photo sensor, the method comprising:

forming a first mask layer on the surface of the substrate for defining positions of a plurality of first doped regions in the photo sensor;

performing a first ion implantation process utilizing second-type dopants to form ~~a plurality~~ the plurality of first doped regions on ~~a surface~~ the surface of the photo sensor;

removing the first mask layer and forming a second mask layer surrounding the photo sensor; and

performing a second ion implantation process utilizing second-type dopants to form a second doped region on the surface of the photo sensor, and the second doped region being overlapped with a partial region of each of the first doped regions.

Claim 2 (original): The method of claim 1 wherein the dopants in the first doped regions and in the second doped region interact with neighboring substrate to form a plurality of depletion regions.

Claim 3 (original): The method of claim 1 wherein the first-type dopants are N-type, and the second-type dopants are P-type.

Claim 4 (original): The method of claim 1 wherein the first-type dopants are P-type, and the second-type dopants are N-type.

Claim 5 (original): The method of claim 1 wherein the substrate further comprises an epitaxial silicon layer, and each of the first doped regions and the second doped region are formed inside the epitaxial silicon layer.

Claim 6 (original): The method of claim 1 wherein a dopant density of the first ion implantation process is less than a dopant density of the second ion implantation process.

Claim 7 (original): The method of claim 1 wherein the surface of the semiconductor wafer further comprises a logic circuit region, and the second ion implantation process forms at least a lightly doped drain (LDD) within the logic circuit region.

Claim 8 (original): The method of claim 1 wherein the method further comprises an annealing process for driving-in the dopants in the second doped region.

Claim 9 (original): The method of claim 1 wherein each of the depletion regions formed between the neighboring first doped regions is a complete depletion region, and a capacitance of each of the depletion regions is approximately equal to zero for increasing a sensing area, decreasing dark current, and further increasing photo current and photon

conversion gain.

Claim 10 (original): The method of claim 1 wherein the second doped region is utilized to be a conducting wire of the photo sensor.